REMARKS

Claims 30 – 33, 35, and 37 are pending. Claims 30, 35, and 37 have been amended. Claims 34 and 36 have been cancelled. No new matter has been added. The applicant respectfully requests reconsideration and reexamination of the application.

In the December 9, 2006 Office Action, the Examiner rejected claims 30 – 37 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 4,924,415 to Winser ("the Winser reference"). This rejection is respectfully traversed in so far as it is applicable to the presently pending claims.

Claim 30 distinguishes over the Winser reference. Claim 30 recites:

> A memory component comprising:
> a random access memory array having a plurality of storage locations;
> **a timing input for receiving a timing signal which when active toggles between first and second states at a periodic rate; and**
> **circuitry, coupled to the timing input and to the random access memory array, for transferring data to the memory component in synchronism with the timing signal and for transferring the data to the random access memory array.**

The Winser reference does not disclose, teach, or suggest the memory component of claim 30. The Examiner states that the CLK signal in the Winser reference is the timing signal and also states that the circuitry for transferring data to the memory component and to the random access memory (RAM) array is described in Fig. 4 and col. 9, lines 21 – 46 of the Winser reference. *(Office Action, page 3)*. The applicants initially note that this disclosure in the Winser reference addresses transferring data out of a RAM array and does not address transferring data into the RAM array, as is recited in claim 30.

The Winser reference discloses that the CLK signal (which the Examiner states is the timing signal) is input into a latch 98 and that the clocked latch is connected to the 24-bit random access data input 100 of the color RAM 96. The Winser reference also discloses that the clocked latches may be constructed using TTL or fast TTL such as Signetics 74374/74F374. *(Winser, col. 9, lines 1 – 3)*. This is not the same as a memory component including **a timing input for receiving a timing signal which when active toggles between first and second states at a periodic rate.** It is not the same because the Winser reference does not disclose that the latch is on the RAM 96 (the RAM 96 being akin to the memory component). In fact, the Winser reference discloses that the color RAMs 96 are VRAM chips (such as the Hitachi HM 53461P-10 VRAM) and does not disclose that the latch is located on the RAM 96 with the RAM array itself. As noted above, the latch of the Winser reference is a separate chip from the VRAM. Thus, the CLK signal of the Winser reference cannot be the timing signal because the RAM, akin to the memory component of claim 30, of the Winser reference (RAM 96) does not receive this signal.

The Winser reference does disclose that the RAM receives a write enable signal (WE2). However, there is no disclosure in the Winser reference that the write enable signal is a signal, which when active, toggles between first and second states at a periodic rate, as is recited in claim 30. Accordingly, applicant respectfully submits that claim 30 distinguishes over the Winser reference.

In addition, the Winser reference does not disclose **circuitry, coupled to the timing input and to the random access memory array, for transferring data to the memory component in synchronism with the timing signal and for transferring**

the data to the random access memory array. As noted above, the latch in the Winser reference lies outside the RAM 96 and associated RAM array. In addition, there is no specific disclosure that the RAM 96 includes circuitry that transfers data into the memory component in synchronism with any timing signal. The Examiner points to a discussion of double buffering in the Winser reference as disclosing the transferring data into RAM array. However, the Winser reference discloses only that the display is refreshed from memory DM1 while the next frame image is being built up in memory DM2. There is no disclosure that the image is being built up in synchronism with a timing signal, as is recited in claim 30. Accordingly, applicants respectfully submit that claim 30 further distinguishes over the Winser reference.

Claims 31 – 33 depend directly on claim 30. Accordingly, applicants respectfully submit that claims 31 – 33 distinguish over the Winser reference for the same reasons as those discussed above in regard to claim 30.

Claim 37 distinguishes over the Winser reference. Claim 37, as amended, recites:

> A memory component comprising:
> a random access memory array having a plurality of storage locations;
> a timing input for receiving a timing signal which when active toggles between first and second states at a periodic rate; and
> **circuitry, coupled to the timing input and to the random access memory array, for receiving data from the random access memory array and for transferring the data from the memory component in synchronism with the timing signal, wherein said circuitry includes a multiplexer.**

The Winser reference does not disclose, teach, or suggest the memory component of claim 37. The Examiner states that the limitation of the circuitry including

the multiplexer is disclosed in the Winser reference by multiplexer 106. *(Office Action, page 4)*. The applicants respectfully disagree. In the Winser reference, the address ALU has two address outputs 102 and 104 which are connected to respective inputs 103 and 105 of an address multiplexer 106. The multiplexer has an address output 107 which is connected to address inputs of the both the Z-Ram 94 and the RAM 96 via a fourth clocked latch. *(Winser, col. 8, line 64 – col. 9, line 1)*. This is not the same as circuitry of a memory component including a multiplexer because the Winser reference is disclosing that the multiplexer is located on a chip separate from the RAM 96. The address information is not even transferred directly to the RAM and stops at an additional chip, i.e., the fourth clocked latch. In addition, the Winser multiplexer is not utilized for receiving data from the RAM array and then transferring data from the memory component, as is recited in claim 37, because the Winser multiplexer is transferring address information, not data. Accordingly, applicants respectfully submit that claim 37 distinguishes over the Winser reference.

Claim 35 depends on the claim 37. Accordingly, applicants respectfully submit that claim 35 distinguishes over the Winser reference for the same reason as discussed above in regard to claim 37.

Dependent claim 33 recites limitations similar to claim 37. Accordingly, applicants respectfully submit that claim 33 further distinguishes over the Winser reference for reasons similar to those discussed above in regard to claim 37.

Applicants believe that the claims are in condition for allowance, and a favorable action is respectfully requested. If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles telephone number (213) 488-7100 to discuss the steps necessary for placing the application in condition for allowance should the Examiner believe that such a telephone conference would advance prosecution of the application.

Respectfully submitted,

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